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Description

METHOD AND SYSTEM FOR DETERMINING MINIMUM POST PRODUCTION TEST TIME REQUIRED ON AN INTEGRATED CIRCUIT DEVICE TO ACHIEVE OPTIMUM RELIABILITY

BACKGROUND OF INVENTION

[0001] Technical Field

[0002] The present invention relates generally to integrated circuit device testing and in particular to post production integrated circuit device testing. Still more particularly, the present invention relates to determining the minimum amount of post production testing required on an integrated circuit device to achieve optimum reliability of that device.

[0003] Description of the Related Art

[0004] A large fraction of the integrated circuits manufactured

today contain some form of defect tolerance or redundancy. Incorporating redundancy into an integrated circuit allows manufacturers to repair many of the defects that would otherwise lead to circuit failures by replacing the defective circuit with a redundant circuit. This can therefore significantly increase the product yield. In memory circuits with redundant memory, for example, it is not uncommon for yields to increase 10 fold when compared to the same circuits containing no redundancy.

[0005] The number of defects that are repaired is of significant interest in areas such as yield modeling, yield learning, reliability estimation and test time reduction. For instance, it is known that as the number of defective elements on an integrated circuit device increases the more likely the integrated circuit device is to fail. Accordingly, the amount of post production test time required to insure an integrated circuit device is reliable increases with the number of defective elements present on the integrated circuit device. Despite this, manufacturers do not currently record this information directly or even attempt to obtain it from repair data.

[0006] Use of a defect count correlates well with a yield/reliability model in which the number of defects a given repaired

chip possesses predicts the chip's probability of failing a reliability test. (See T.S Barnett, A.D. Singh, M. Grady, K.G. Purdy, "Redundancy Implications for Product Reliability: Experimental Verification of an Integrated Yield Reliability Model", Proceedings 2002 International Test Conference, October 2002, to appear).

[0007] A paper presented at the IEEE International Test Conference in 2001, titled "Estimating Burn In Fallout for Redundant Memory", authored by T.S. Barnett, et al, describes how the number of repaired defects can be used to estimate the early life reliability of redundant memories. The paper "Yield Reliability Modeling for Fault Tolerant Integrated Circuits" by T.S. Barnett et al., (Proceedings of Defect and Fault Tolerance, October, 2001), extends this approach to more general fault tolerant architectures. While these works demonstrate how one could exploit defect count information for the purpose of early life reliability prediction, no specific technique for obtaining defect counts from integrated circuits is discussed. It would be desirable, therefore, to provide a mechanism for automatically counting defective cells and active elements with defective cells in order to the minimize the amount of post production testing required on an integrated circuit

device to achieve optimum reliability of that device.

Summary of Invention

[0008] It is therefore one object of the present invention to provide improved integrated circuit testing.

[0009] It is another object of the present invention to provide improved post production testing for integrated circuit devices.

[0010] It is another object of the present invention to minimize the amount of post production testing required on an integrated circuit device to achieve optimum reliability of that device.

[0011] The foregoing objects are achieved as is now described. A counter is added to built in self test circuits on integrated circuit devices and is incremented each time a defective cell or an active element with a defective cell is detected on an integrated circuit device. The output of the counter is made available to a system that analyzes the number of defective cells or active elements with defective cells relative to normalized numbers for that integrated circuit device lot and determines the minimum amount of post production test time required on an integrated circuit device to achieve optimum reliability of that device.

[0012] Alternatively, the information about defective cells or ac-

tive elements with defective cells (DFECTS) that is made available to an external device, such as a laser fuse tool, is provided to a system that analyzes the number of DEFECTS relative to normalized numbers for that integrated circuit device lot. The system then determines the minimum amount of post production test time required to achieve optimum reliability for said integrated circuit device.

[0013] The above as well as additional objectives, features, and advantages of the present invention will become apparent in the following detailed description.

Brief Description of Drawings

[0014] The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0015] FIG. 1 is a schematic representation of an integrated circuit device comprising one or more active elements, a built in self test circuit, and a counter circuit.

[0016] FIG. 2 is a high level logic flow chart of the on-chop

counter process used to determine the minimum amount of post production testing required on an integrated circuit device to achieve optimum reliability of that device with a counter circuit.

[0017] FIG. 3 is a high level logic flow chart of the off-chip count process used to determine the minimum amount of post production testing required on an integrated circuit device to achieve optimum reliability of that device.

[0018] FIG. 4 is a schematic representation of an integrated circuit device comprising one or more active elements, each containing its own built in self test circuit with a counter which is daisy chained to the counter of the adjacent active element.

[0019] FIG. 5 is a high level block diagram of the integrated circuit of Figure 4.

[0020] FIG. 6 is a high level logic flow chart of the multiple on-chip counter process.

[0021] FIG. 7 is a high level logic flow chart for the determine minimum test time process used in determining the minimum amount of post production testing required on an integrated circuit device to achieve optimum reliability that device.

DETAILED DESCRIPTION

[0022] With reference now to the figures, and in particular with reference to Figure 1, there is depicted an integrated circuit device 100 as one embodiment of the present invention. Integrated circuit device 100 includes a built in self test (BIST) circuit 110 that is directly coupled to counter 120 so that it can be incremented each time BIST circuit detects a DEFECTS. Each active elements 150(a) 150 (n) may contain one or more cells, any of which may be defective. The counter is coupled to output port 140 so that the count is accessible to determine a minimum post production test time required on an integrated circuit device to achieve optimal reliability of that device. BIST circuit 110 is also coupled to BIST interface 130. Active elements 1 through n 150(a) 150(n) are coupled to the BIST interface 130 to make it possible for BIST circuit 110 to access each active element 150(a) 150(n). Those with ordinary skill in the art would recognize that active elements could be memory modules, processor modules, controller modules, or any other electronic module.

[0023] Referring now to Figure 2 that depicts a high level logic flowchart of an on-chip counter process 200. The first step in the process is to test the next active element for defective cells 210. If one or more DEFECTS are detected

220 in the active element, then a counter is incremented 230. If a defect is not detected, this step is bypassed and the next step is to determine if all active elements are now tested. 240. If they are, the count of DEFECTS is available 250 to determine minimum post production test time required on an integrated circuit device to achieve optimum reliability of that device. If they are not, the next step is to return to test the next active element 210 and repeat the foregoing process until all active elements have been tested.

[0024] Another embodiment of the present invention may incorporate banks of metal fuses on the integrated circuit device. A laser tool is then used to delete some of the fuses on the integrated circuit device. These fuses are connected to a circuit on the integrated circuit device that discerns the presence or absence of the fuse. Presence of a fuse indicates to the integrated circuit device that the redundant element should be used. Absence of a fuse similarly, indicates to the integrated circuit device that the redundant element should not be used. The presence and absence of fuses is also translated into a code that indicates to the integrated circuit device which element of the integrated circuit is to be replaced by the redundant ele-

ment. One of ordinary skill in the art will recognize that this is just one method of creating redundancies on integrated circuit devices. Other methods of redundancy will provide similar defect count information that may be used to determine minimum test times.

[0025] Figure 3 depicts a high level logic flowchart of such an off-chip counter process 300. The first step is to intercept instructions routed to a laser fuse tool 310 used to delete fuses on the integrated circuit device. Then the number of "enable fuse" bits that remain are counted 320. Since each one of these corresponds one to one with a redundant element replacement, this count represents the number of DEFECTS on the integrated circuit device. This count is made available to determine the minimum amount of post production test time required on an integrated circuit device for optimal reliability of that device.

[0026] The intercepted instructions in this embodiment may also be used to identify more information that just the number of DEFECTS. A fuse design may be employed that may determine the location of the DEFECTS. Post production test time may then be more accurately determined by analyzing the physical proximity of DEFECTS. For instance, instead of a single fuse for each redundant element, there

could be nine fuses. The first would be an enable bit and the remaining eight fuses representing the logical address of the active element with defective cells that is being replaced. Since the laser tool would receive instructions regarding the enable bit fuse and the eight address fuses, the addresses can be intercepted as well as the count. As a result, the physical location of DEFECTS is known based on the logical address. If the DEFECTS are close together in physical proximity, then more post production testing might be required on an integrated circuit device to achieve optimum reliability of that device. The proximity of DEFECTS along with the count of DEFECTS will be used together to determine a minimum post production test time.

[0027] Now referring to Figure 4, there is depicted an integrated circuit device 200 in another embodiment of the present invention. Integrated circuit device 400 includes active elements 420(a) 420(n). Each active element 420(a) 420(n) contains a BIST and is coupled to its own individual count register 410(a) 410 (n). Each count register 410(a) 410(n) is coupled to the next count register 410(a) 410(n). The final count register 410(n) is coupled to an accumulator 440, which is coupled to count register 410(a). This con-

figuration allows the count in each count register 410(a) 410(n) to be shifted to and accumulated in accumulator 440 such that the total count from all count registers 410(a) 410(n) is available at output port 430. This configuration also allows the original count in each count register to be preserved because it is shifted back into the count register during the accumulation process. Thus, if a particular active element count needs to be utilized to determine the minimum post production test time required on an integrated circuit device to achieve optimum reliability of that device, it is available at output port 430. . Those with ordinary skill in the art would recognize that active elements contain one or more cells and could be memory modules, processor modules, controller modules, or any other electronic module.

[0028] Figure 5 depicts a high level block diagram of the integrated circuit device shown in Figure 4. A repair count register 520(a) 520(n) is added to the BIST engine of each memory 510(a) 510(c) on the integrated circuit to store the number of repairs. Each repair count register 520(a) 520(n) is daisy chained to the next repair count register 520(a) 520(n) on the chip, and connected to the main fuse controller 500. The main fuse controller 500 alternately

shifts and accumulates the repair count from each of the repair count registers 520(a) 520(n) until the total repair count is accumulated. As the data is shifted into the main fuse controller 500, the main fuse controller 500 shifts the data back into the repair count registers 520(a) 520(n) so that they are each returned to their original state. This allows for the counts to be output at the end of the entire sequence, such that individual memory fail counts are available via an output pin 530.

[0029] Referring now to Figure 6, a high level logic diagram of the multiple on-chip counter process 600. In the first step, DEFECTS are counted in the next active element 610 and the number is deposited in the count register. The next step checks to see if the DEFECTS have been counted in all of the active elements 620. If they have not, the process returns to count the DEFECTS in the next active element 610. If they have, then the next count is shifted into the accumulator 630 from the count register. The count is added to the accumulated value in the next step 640. The next step is to determine if all counts from all active elements have been shifted into the accumulator 650. If they have not, the process returns to shift in the next count 630. If they have then the final step is to shift the last

count in the accumulator out 660, so that all count registers contain their original number.

[0030] Referring now to Figure 7, that is a high level logic flowchart of the determine minimum test time process 700. In the first step, DEFECTS count is compared to a predetermined count A 710. This predetermined count could be determined as a result of analysis of wafer or die lots. The predetermined count could also be updated in real time to reflect a trend in DEFECTS counts. If it is less than or equal to A, then the minimum test time is a predetermined amount AA 720. The predetermined test time may also be updated in real time to reflect a trend in active element with defective cell counts. It could also be determined as a result of analysis of wafer or die lots. If it is not less than or equal to A, then DEFECTS count is compared to B to determine if it is less than or equal to B 730. If it is, then the minimum test time is BB. This comparison test is completed for up to N times, where N is the number of different levels of predetermined minimum test times based on defect counts 750. If there are too many defects, the integrated circuit device may be discarded 770. One of ordinary skill in the art would recognize that there is a plurality of methods that could be employed to

determine the incremental defect counts and the subsequent minimum amount of post production test time required to achieve optimal reliability of that device.

[0031] While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.